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ISSN 2249-3352 (P) 2278-0505 (E)
Cosmos Impact Factor-5.86

An ALU architectural solution that is efficient for low power Internet of Things applications

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Abstract:

An effective logic design for a processor architecture focused on the Internet of Things (IoT) was suggested in this study. The control panel is used in the IoT board, and it is obvious that the Arithmetic Logic Unit (ALU) is a major block in almost all activities. In order to reduce the amount of switching and optimize the architecture-level selection of operations,

the suggested ALU architecture makes use of a gray coding approach (CGGC) in conjunction with clock gates. The present design was created on the Vivado 16 simulation platform using verilog code. Reduced LUTs by 18%, low power consumption, and optimum resource utilization—all of which are sought after in IoT applications—describe the enhanced performance of the altered design.

Keywords:

Vivado, Clock Gating, Gray Coding, ALU, and Verilog

I. INTRODUCTION

In 1971, Intel developed the Intel 4004, the first semiconductor microprocessor with four bits of data handling capability. Today, 64-bit and more powerful high-end central processing units (CPUs) and controllers are ubiquitous. At the moment, the frequency was somewhere between megahertz and gigahertz. This work will only become practicable when CMOS technology advances, which increases in tandem with the density of devices on silicon wafers.

Be receptive to low-energy research, nevertheless, since this raises the problem of excessive energy usage. Numerous research and methodologies have been proposed in the literature so far to increase wafer energy efficiency [1]. Three solutions have been proposed to reduce power consumption: the use of gate clocks, block devices, and heartbeats. There are three different kinds of clock gates that have been suggested, each with its own set of measurements: latch-based clock gate systems, flip-flop clock gates, and latchless clock gates [2]. It is also evident from the reduction in energy leakage that the amount of active sites influences energy leakage [3]. Here are two optimization strategies that may be used to change the time measurements.

These methods may be used as a post-processing strategy in wearable devices [4]. In contrast to the second set, which has a huge clock and looks like a door clock, the first provides an approximate time. Everyone knows about ALU on FPGA and how it works. It also shows that the low power consumption solution is comparable to clock gating in terms of performance.

Most people imagine a tiny circuit when they hear the terms "microprocessor" or "microcontroller," but in fact, the ALU on the chips is responsible for processing data and performing operations like arithmetic and logic. Modern high-end

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ISSN 2249-3352 (P) 2278-0505 (E)
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microprocessors come with an ALU pipeline design that increases power consumption but improves chip performance. Therefore, this study aims to provide an improved design for a low-power ALU. One structure is planned to have no clock pulse at all, whereas the other has a gated clock pulse. Both designs have undergone testing for a range of procedures at separate periods.

II. Proposed Architecture

The First Method: Clock Gating Dissipation of static power occurs while the ALU is off and dynamic dissipation occurs when the ALU is active. The input switching activity contributes the majority of the power.

Controlling the clock on it efficiently optimizes the dynamic power dissipation. One way to reduce dynamic power usage is to momentarily disable modules that are not in use or inactive components. One way to control the flow of data updates via a potential unit is to use a clock gate to filter out updates to units whose output isn't required. Figure 1 displays the circuit that uses a gated clock to operate a D flip-flop. It is possible to activate all of the flip-flops at once using the clock signal. Unless the selection signal clock is set, the content remains constant.

In such case, a new input is created by combining the values in the data registers. Clock gating creates a gated clock signal by using the "EN" signal to gate the clock signal [5].

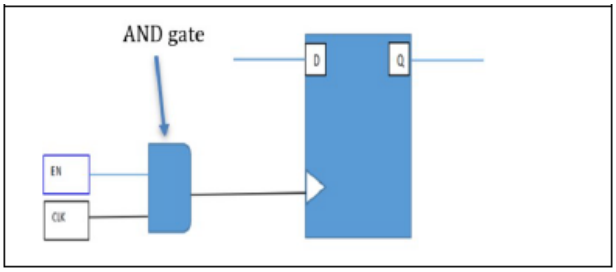

Fig 1. Gated clock design

Section B: Gray Coding Method A system of modified binary numerals known as "gray coding," sometimes termed "Gray binary code" or "reflected binary code," differs from the traditional binary representation.

Gray coding is useful for rotary encoders and communication systems because it simplifies electrical circuits and decreases mistakes due to the one-bit difference between subsequent values.

Grey coding ensures minimal variations between adjacent values, in contrast to typical binary representations that permit substantial fluctuation between two successive numbers [6]. Error detection and repair benefit greatly from this unique quality since it lessens the likelihood of misunderstanding [7]. Gray coding is an essential tool for digital technology that ensures data is accurate and reliable.

Table 1.1 : Logical and Arithmetic Operations

Operations	Opcode
Clear	0000
Return b	0001
Compliment b	0010
Return a	0011
Increment	0101
Decrement	0110
Left shift	0111
Add	1000
Subtract	1001
Add with carry	1010
Subtract with carry	1011
And	1100
Or	1101
Xor	1110
Xnor	1111

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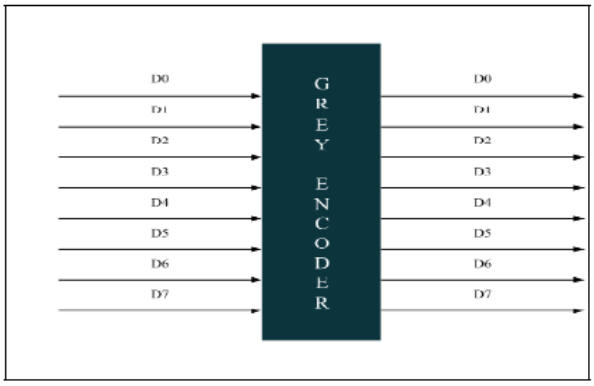

Fig 2 Gray Encoder(8 bit)

The ALU design consists of two eight-bit function components, "a" and "b," and one four-bit decision input, "SEL." For example, the ALU may perform the arithmetic and logic operations outlined in Table 1.1. With the "SEL" line's selected function, doing operations "a" and "b" with 8 bits each will make the result seem larger than 8 bits. There are 16 items in the output "Y," which contains the outcomes such as "clear," "return," "complement," "increment," "decrement," "add," and so on.

C.Alu Creative See the ALU's internal blocks in Fig. 3. A single 8-bit operand, a, and a single 8-bit control signal, clk, are the inputs of each ALU operation block [8]. All of the operating blocks are connected to the input of a multiplexer that has numerous inputs and outputs. The multiplexer has 8 bits for each input and 8 bits for each output. An already-started processor operation may be selected using the multiplexer's 4-bit choose input [9]. Although it works well for most CPU architectures, the aforementioned design does have a downside. The results of the simulation are shown in Figure 4, and

Fig 5 shows the schematic block from the s/w platfom.

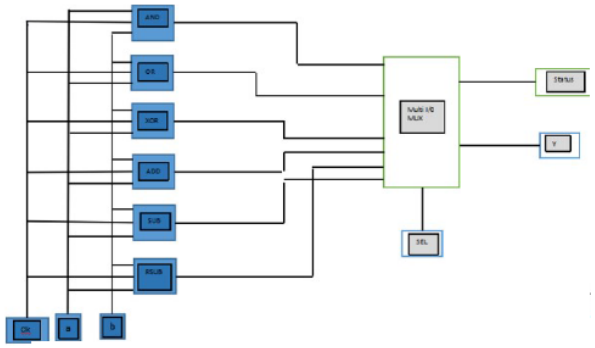

Fig 3 Block diagram of normal ALU

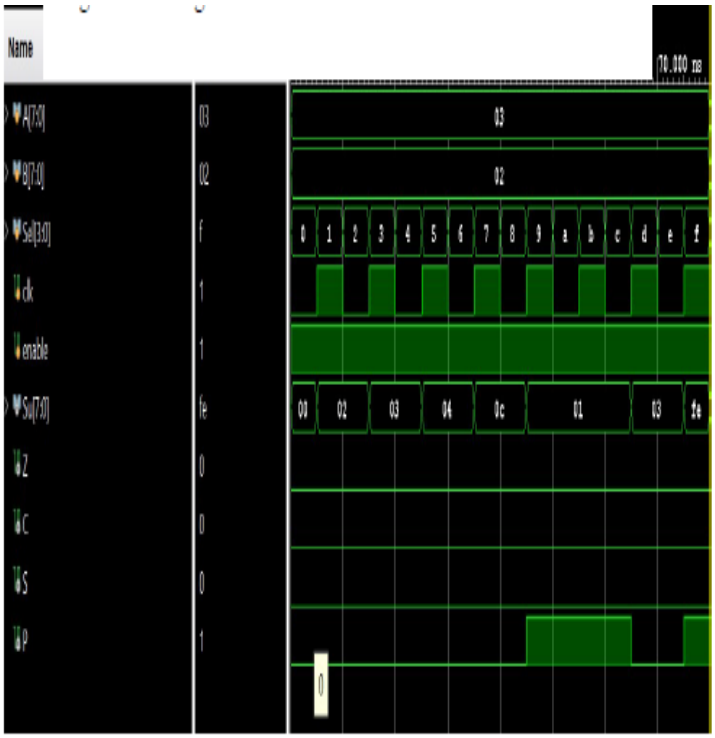

Fig 4 Simulation of ALU in vivado

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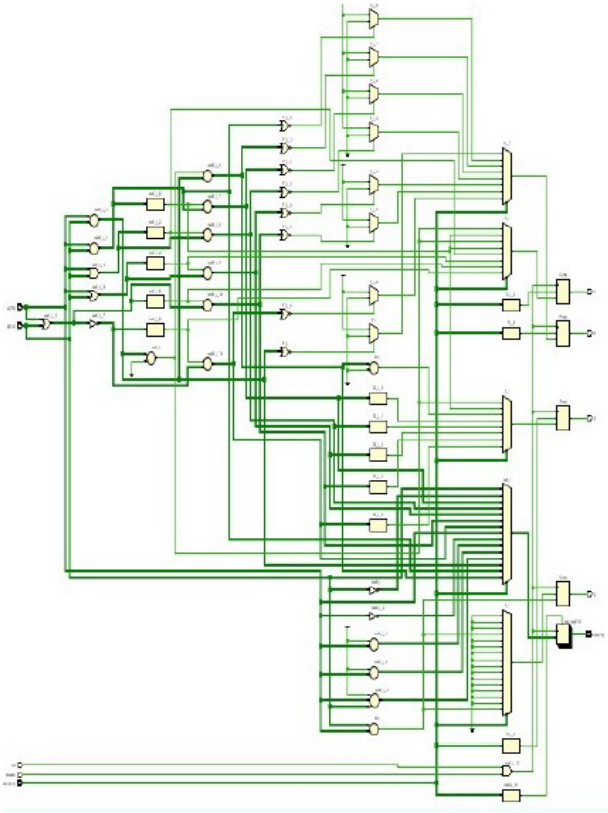

Fig 5 RTL Schematic of normal ALU

Revised ALU Subunit We unnecessarily boost switching activity at the input of blocks that aren't now engaged since the clk is continually available to all operational blocks. Because of this, the chip's power consumption and switching activity will both rise. The ALU can only process the choose input for a single operation at a time since each ALU operation is its own independent operation. By disabling the clock of operational blocks that aren't currently doing the selected operation, it is possible to reduce switching activity [11]. Figure 6 shows the ALU's power-efficient design, which is a combination of clock gating and gray coding (CGGC). Figure 7 displays the results of the ALU, gating, and coding principle construction. The updated CGGC architecture is schematically shown in Fig. 8. In Table 1.2, we can see the results of our comparison of the two designs.

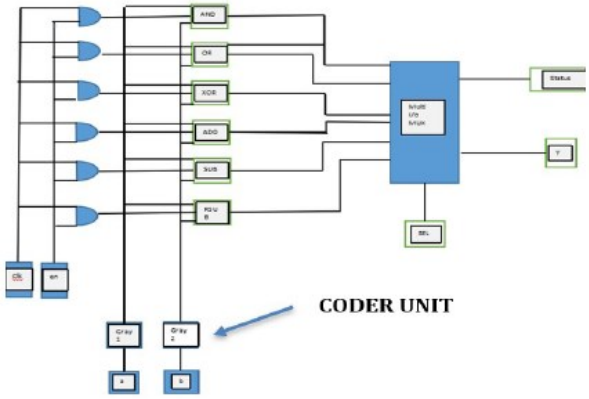

Fig 6 Block diagram of modified ALU

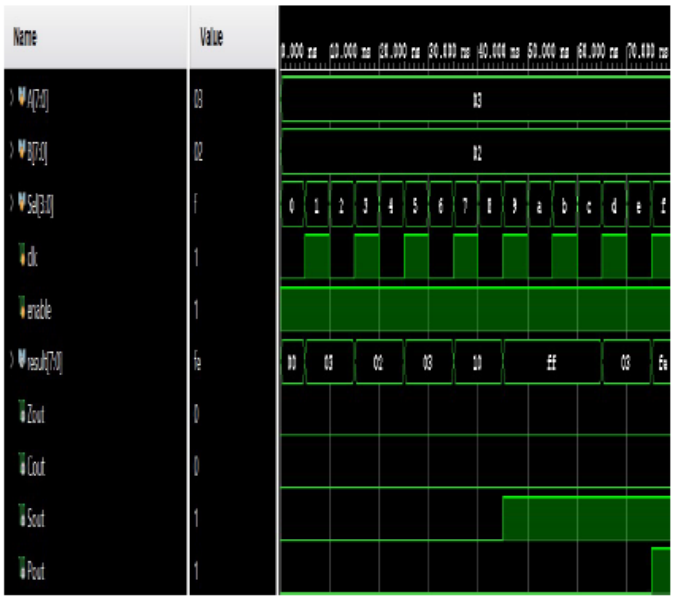

Fig 7 Simulation of modified ALU in vivado

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Table 1.2 Device Summary			
Parameters	Normal ALU	Proposed ALU(CGGC)	Resource of saving
LUTs	164	136	17%
FFs	12	11	8%
I0s	50	48	4%

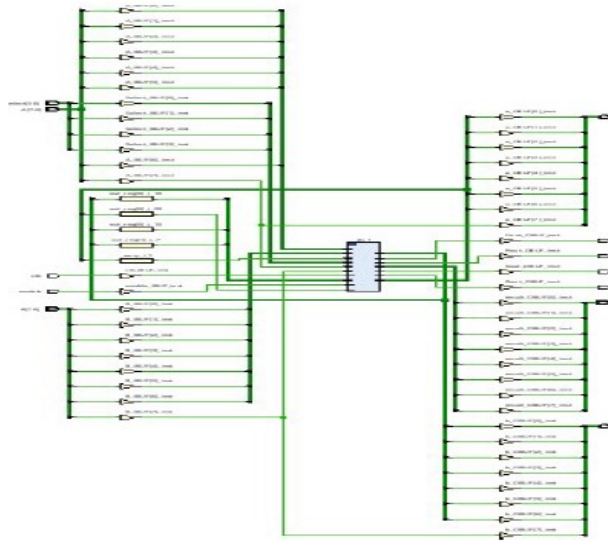

Fig 8 RTL of modified ALU in vivado

V. Conclusion

The proposed clock gated ALU architecture drastically cuts power consumption owing to lower utilization of LUTs slices, flip-flops, and IOs, which is especially helpful for newer high-end processors that operate at higher frequencies. Based on the analytics, the updated CGGC architecture improves performance by delivering a 16% reduction in power consumption caused by Look Up Table utilization. In addition, the number of flip-flops and Ios in the revised design is somewhat lower. This proves that the altered ALU design for low power applications is compatible with both high-end and low-end CPU architectures used in IOT devices.

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